REMARKS

This paper is submitted in response to the Examiner's Action dated 4 May 2005, having a shortened statutory period set to expire on 4 August 2005. In responding to the Action of 4 May 2005, Applicants have not amended the claims.

I. Telephone Communications

Applicant appreciates the courtesies extended by the Examiner in the series of phone messages exchanged between 4 May 2005 and 4 August 2005, and in telephone communications preceding Applicant's response of 17 March 2005. Applicant thanks the Examiner for her patience and courtesy in all communications related to this case.

II. Introduction to Rejections under 35 U.S.C. § 103

In the present Office Action, Claims 1, 7 and 10-27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,873,630 to Muller *et al.* (*Muller*) in view of U.S. Patent No. 6,389,000 to Jou (*Jou*). Those rejections are most respectfully traversed in view of the discussion made herein, and favorable reconsideration of the claims is requested.

III. The 'dual-port memory' of exemplary Claim 1 is not taught or suggested

First, with respect to exemplary Claim 1, Applicant most respectfully submits that the cited combination of references does not teach or suggest Applicant's claimed feature of "a controller for controlling said memory and said interfaces and for monitoring a data rate of said data between said memory and said plurality of links, wherein said controller includes means for cyclically distributing data to be communicated from said memory to said second device among said low-speed interfaces, such that each of said plurality of low speed interfaces receives a number of consecutive units of said data equal to the numerator of its associated fraction". The Examiner asserts at paragraph two that "Muller discloses ... a controller for controlling said memory and said interfaces and for monitoring a data rate of said data between said memory and said plurality of links, wherein said controller includes means for cyclically distributing data to be communicated

from said memory to said second device among said low-speed interfaces, such that each of said plurality of low speed interfaces receives a number of consecutive units of said data equal to the numerator of its associated fraction". The Examiner cites *Muller* at Column 5, lines 37-46 and Column 7, lines 15-25, as teaching this functionality. Cited text of Column 5 of *Muller* discloses:

> During operation of the embodiment depicted in **FIG. 1**, distributor/collector **100** receives frames, or packets, from a Medium Access Control (MAC) layer through 10GMII **102** at a rate in excess of 1 Gbps (e.g., up to approximately 10 Gbps in the illustrated embodiment). Similarly, distributor/collector **100** operates in the reverse direction to provide a MAC layer with reconstructed frames at the same rate of transfer. This transmission rate is approximately equal to the sum of the rates at which data are transferred across the 2GMII interfaces that connect distributor/collector **100** to each PCS. Thus, in FIG. **1**, each 2GMII may operate at a rate of approximately 2.5 Gbps.

And the cited text of Column 7 discloses:

> In order for the combined 2GMIIs to carry the same amount of data as 10GMII **202**, each 2GMII, including 2GMII **208a**, may operate at the same signaling rate as 10GMII **202**. The same clock frequency used by 10GMII 202 (e.g., 156.26 MHz), again sampled on both edges, may be used to achieve the necessary 312.52 MBd signaling rate. During operation of this embodiment, therefore, each 2GMII may carry approximately 1/N of the information carried on 10GMII 202, where N is the number of channels. In the illustrated embodiment in which four logical channels are depicted, 2GMII 208a and the other 2GMIIs each carries approximately 2.5 Gbps in each direction.

Having reviewed the cited references, Applicant most respectfully submits that the cited texts do not teach or suggest "a controller for controlling said memory and said interfaces and for monitoring a data rate of said data between said memory and said plurality of links, wherein said controller includes means for cyclically distributing data to be communicated from said memory to said second device among said low-speed interfaces, such that each of said plurality of low speed interfaces receives a number of consecutive units of said data equal to the numerator of its associated fraction", as is recited in amended exemplary Claim 1. More specifically, the cited passage from *Muller* does not teach a variable numerator, irreducible or otherwise. Instead,

Muller discusses operations on a variable denominator, wherein each fraction is a 1/N expression, and the numerator is fixed. Nor does *Muller* address assignment of consecutive units.

IV. The 'dual-port memory' of exemplary Claim 1 is not taught or suggested

First, with respect to exemplary Claim 1, Applicant most respectfully submits that the cited combination of references does not teach or suggest Applicant's claimed feature of "a dual-port memory for storing data". The Examiner asserts at paragraph two that "Muller discloses ... a dual-port memory for storing data". The Examiner cites *Muller* at Column 4, lines 12-16, as teaching this functionality. Cited text of *Muller* discloses:

> The presently described embodiment achieves a high data communication rate (e.g., 10 Gbps) by dividing, or striping, a data stream directed from one network entity to another network entity into multiple logical channels.

Having reviewed the cited references, Applicant most respectfully submits that the cited texts do not teach or suggest "a dual-port memory for storing data", as is recited in amended exemplary Claim 1. More specifically, the cited passage from *Muller* does not teach or suggest any memory, dual-port or otherwise. In fact, neither the word 'memory' nor the word 'port' appears anywhere in the text of *Muller*.

V. The 'high-speed interface' of exemplary Claim 1 is not taught or suggested

Still with respect to Claim 1, Applicant respectfully submits that the cited combination of references does not teach or suggest Applicant's claimed feature of "a high-speed interface for transmitting said data between a first device and said dual-port memory, wherein said high-speed interface communicates data at an initial rate", as recited in Applicant's exemplary Claim 1. The Examiner cites *Muller* at Column 5, lines 8-16, and Column 8, lines 5-12 as teaching the recited functionality. The text of Column 5, lines 8-16 of *Muller* discloses that:

> A physical layer device in architecture **120** may be viewed to encompass entities corresponding to a PHY of architecture **130** (i.e., Physical Coding Sublayer, Physical Medium Attachment, Physical Medium Dependent), except that they must operate at higher rates in order to transmit and receive multiple gigabits of information per second. A PHY of architecture **110** may also encompass similar entities, plus distributor/collector **100**. Although architecture **110** comprises four separate PHYs in **FIG. 1**, any number may be implemented in alternative embodiments of the invention. As will be discussed in more detail below, the number of PHYs may be a factor in determining the number of logical channels employed by a high-speed Ethernet interface device according to an embodiment of the invention.

Further, the text of Column 8, lines 5-12 of *Muller* discloses that:

> As described previously, an embodiment of the present invention achieves a high data transfer rate (e.g., approximately 10 Gbps) by striping data across multiple logical channels. However, embodiments of the invention are also compatible with high-speed Ethernet interfaces that communicate across single channels. Naturally, however, such single channels must operate at higher data transfer rates than multiple channels that act cooperatively.

The Examiner asserts that "Muller discloses ... a high-speed interface for transmitting said data between a first device and said dual-port memory, wherein said high-speed interface communicates data at an initial rate" Having reviewed the cited references and the reasoning of the Examiner, Applicant most respectfully submits that the cited texts do not disclose "a high-speed interface for transmitting said data between a first device and said dual-port memory, wherein said high-speed interface communicates data at an initial rate" because the cited text makes no mention of interaction with a dual port memory.

VI. No specific teaching of a motivation to combine is cited with respect to Claim 1

As set forth in MPEP § 2143, the first criterion for establishing a *prima facie* case of obviousness is that "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to...combine reference teachings." In evaluating motivation or suggestion to combine reference teachings, "a prior art reference must be considered in its entirety, i.e., as a whole" (emphasis in

original). MPEP 2141.02, citing *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir 1983) *cert. denied*, 469 U.S. 851 (1984). In view of the teachings of the references as taken as a whole, Applicant respectfully submits that there is no objective suggestion or motivation in the cited references (or generally in the art) that would lead a skilled artisan to combine the reference teachings to obtain the present invention. If such suggestion or motivation existed, the Examiner would have, no doubt, cited by column and line number a passage in one of the references cited or a well known teaching in the art to discharge his duty to "explain why the combination of the teachings is proper." MPEP 2142, citing *Ex parte Skinner*, 2 USPQ2d 1788 (Bd. Pat. Appl & Inter. 1986). At page 3 of the present office action, the Examiner asserts that:

> Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to incorporate or implement Jou's controller in Mueller's device in order to transmit data at a particular rate.

Because the Examiner's combination of references is not supported by any objective teaching in the references or art, Applicant believes that the examiner has failed to establish a *prima facie* case of obviousness.

VI. Arguments with respect to Claim 1 apply broadly

Applicant respectfully submits that the rejection of exemplary Claim 1 under 35 U.S.C. § 103 is overcome. The foregoing arguments made with respect to Claim 1 are also made with respect to Claims 7 and 10-27.

VIII. The "modem" of Applicant's Claim 7 is not taught or suggested

With respect to exemplary Claim 7, Applicant most respectfully submits that the cited combination of references does not teach or suggest Applicant's claimed feature "wherein at least one of the set of said high-speed interface and said plurality of low speed interfaces comprises means for establishing a connection with a modem", as recited in Applicant's exemplary Claim 7. The Examiner asserts that *Muller* teaches "wherein at least one of the set of said high-speed interface and said plurality of low speed interfaces comprises means for establishing a connection with a modem", at Column 4 , lines 20- 25. The cited text of *Muller* discloses:

> For example, a single physical link may be configured to use frequency division multiplexing (FDM) or wave division multiplexing (WDM) in order to carry the logical channels over one electrical or optical conductor. Alternatively, two or more separate physical conductors may be employed. In one particular embodiment, each logical channel is carried by a separate physical conductor, such as individual fiber-optic strands in a fiber bundle or ribbon, or as a separate wireless signal.

Having examined the cited text, Applicant most respectfully submits the word "modem", does not appear in the cited text of *Muller*, or anywhere else within the reference. Applicant most respectfully submits that the Examiner has not shown any teaching or suggestion modem, much less Applicant's claimed feature of "wherein at least one of the set of said high-speed interface and said plurality of low speed interfaces comprises means for establishing a connection with a modem". Applicant respectfully submits that the combination of references does not teach or the claimed functionallity. Applicant respectfully submits that the rejection of Claims 4-6, 12-14, and 20-22 under 35 U.S.C. § 103 is overcome.

CONCLUSION

Applicants respectfully submit that all Claims are now in condition for allowance. Because the amendments and arguments overcome the claim rejections, Applicants respectfully request issuance of a Notice of Allowance for all claims now pending.

No additional fees are believed to be required; however, in the event that additional fees are required, please charge any other fees necessary to further the prosecution of this application to **IBM CORPORATION'S Deposit Account No. 09-0457.**

Applicants respectfully request the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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